What is claimed is:

1. An early-late pulse accumulator comprising:

a first logic device configured to toggle a first output logic level upon receipt of an early pulse;

a second logic device configured to toggle a second output logic level upon receipt of a late pulse, wherein the first and second logic devices are configured to allow only one of the first and second output logic levels to be toggled at a time;

a first ripple divider configured to receive the first output logic level and to provide a scaled down count of the number of times the first logic device toggles;

a second ripple divider configured to receive the second output logic level and to provide a scaled down count of the number of times the second logic device toggles;

a first synchronizing logic device configured to receive the scaled down count of the number of times the second logic device toggles and to generate a first terminal count signal proportional to the number of early pulses received by the first logic device;

a second synchronizing logic device configured to receive the scaled down count of the number of times the second logic device toggles and to generate a second terminal count signal proportional to the number of late pulses received by the second logic device; and

an integrator configured to receive the first and second terminal count signals and generate a net early-late count.

2. The accumulator of claim 1 wherein the integrator is configured to increment upon receipt of the first terminal count signals and decrement upon receipt of late terminal count signals.

3. The accumulator of claim 1 wherein the first logic device comprises a first XOR gate configured to toggle a first flip-flop, and wherein the second logic device comprises a second XOR gate configured to toggle a second flip-flop.

4. The accumulator of claim 1 wherein the first logic device and the second logic device are configured to toggle as clocked by a transition in the data signal.

5. The accumulator of claim 4 wherein the transition in the data signal is a rising data signal.

6. The accumulator of claim 4 wherein the transition in the data signal is a falling data signal.

7. The accumulator of claim 4 wherein the transition in the data signal comprises an alternating rising data signal and falling data signal.

8. A pulse accumulator comprising:

a logic device for receiving more than one early pulse and more than one late pulse;

an early ripple divider configured to count the early pulses on a scaled down basis;

a late ripple divider configured to count the late pulses on a scaled down basis;

an early pulse synchronizing device configured to receive the scaled down early pulses and to generate an early terminal count corresponding to the number of early pulses;

a late pulse synchronizing device configured to receive the scaled down late pulses and to generate a late terminal count corresponding to the number of late pulses;

an integrator configured to increment upon receipt of the early terminal count signals and decrement upon receipt of the late terminal count signals.

9. A method for synchronizing an output signal to a data signal, the method comprising the steps of:

receiving a data signal at a phase detector;

receiving an output signal at the phase detector;

comparing the data signal and the output signal in the phase detector;

generating, in the phase detector, a timing signal indicating the relative phase relationship between the data signal and the output signal;

dividing the timing signal to generate a scaled down timing signal;

receiving the scaled down timing signal at an integrator; and

generating in the integrator a control signal for modifying the output signal to synchronize the output signal to the data signal.

10. The method of claim 9 wherein the data signal has an associated data signal phase, the output signal has an associated output signal phase, and wherein the comparing step further comprises comparing the data signal phase with the output signal phase and generating a late pulse for each data signal phase lagging the output signal phase, and generating an early pulse for each data signal phase leading the output signal phase.

11. The method of claim 9 wherein the timing signal comprises early pulses and late pulses and wherein the dividing step further comprises the step of generating a scaled down early count and a scaled down late count; and wherein the generating step further comprises the integration of the scaled down early and late counts.

12. A system for synchronizing a recovered clock signal to a data signal comprising:

a phase detector configured to receive an input data signal and a recovered clock signal, wherein the input data signal has an input data signal phase and the recovered clock signal has a recovered clock signal phase, the phase detector further configured to compare the input data signal phase to the recovered clock signal phase and to provide an early pulse for each input data transition where the recovered clock phase leads the data signal phase and a late pulse for each input data transition where the recovered clock phase lags the data signal phase;

a pulse accumulator configured to receive the early and late pulses, and to provide a scaled down early pulse signal and a scaled down late pulse signal; and

an integrator configured to receive the scaled down early and late pulses and to create a control signal for synchronizing a recovered clock signal to a data signal.

13. The system of claim 12 further comprising a phase selector configured to select a signal phase from among more than one signal phases provided by a voltage controlled oscillator, wherein the phase selector is configured to vary the frequency of the recovered clock.

14. The system of claim 12 further comprising a phase selector configured to select a signal phase from among more than one signal phases provided by a voltage controlled oscillator, wherein the phase selector is configured to vary the phase of the recovered clock.

15. The system of claim 12 further comprising a phase selector configured to select a signal phase from among more than one signal phases provided by a voltage controlled oscillator, wherein the phase selector is configured to vary the frequency and phase of the recovered clock.

16. A delayed lock loop device comprising:

a phase detector configured to compare a reference signal and a clock signal, to provide an early pulse signal for each reference signal phase lagging the clock signal phase, and to provide a late pulse signal for each reference signal phase leading the clock signal phase;

a pulse accumulator configured to receive an early pulse signal and a late pulse signal from the phase detector and to provide a scaled down accumulation of early and late pulse signals; and

an integrator configured to receive the scaled down accumulation of early and late pulse signals from the pulse accumulator and to generate a control signal for use in aligning a clock signal to a data signal.